**Max Score = 15 points**

CS 250 2018 Spring Homework 03

This assignment is due at 11:59:00 pm Thursday, February 01, 2018.

Upload your typewritten answer document in either PDF or Word format to Blackboard.

Download from Blackboard to be sure that your upload was successful. Your last upload that is not marked “LATE” by Blackboard is the upload that will be graded. There is no “grace” period for late uploads.

1. What sequence of commands to an S'R' latch will certainly produce a falling edge on the latch output Q?

If S’ changed from 0 to 1 and R’ changed from 1 to 0

1. Regarding the decoder and ripple-carry adder.
   1. What is the number of gates required to construct a 5x32 decoder?  
      37

5 to get inverted values of inputs and 32 to represent different outputs

* 1. In units of gate delays, what is the propagation delay of the decoder?  
     1\*(5 NOT delay + 1 AND delay)

5\*(4 NOT delay + 1 AND delay)

10\*(3 NOT delay + 1 AND delay)

10\*（2 NOT delay + 1 AND delay）

5\*(1 NOT delay+ 1 AND delay)

1\*AND delay

* 1. How does this compare to the number of gates needed to build a 5-bit ripple-carry adder, an adder that accepts inputs represented using 5 bits, and to the propagation delay of the ripple-carry adder?  
     Number of gates 5\*5=25

Propagation delay 2\*5+2 = 12

* 1. What is the ratio of the propagation delay of the decoder to that of the adder?

Gate ratio: 25/37

Delay ratio: 1/12

1. Fill in the following table to show how the given meaningless bit string is interpreted according to each of the six data representations: unsigned integer, sign magnitude, 1’s complement, 2’s complement, packed BCD, and ASCII character.  
   Express your answers using base 10 digits, hexadecimal notation, or ASCII character, whichever is most appropriate. Show a + sign or a – sign as appropriate for zero values when the representation permits both possibilities. If the bit string does not have a valid interpretation for a given representation, write “Error” in the space provided.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Bit string | Unsigned integer | Sign magnitude | 1’s comp-lement | 2’s comp-lement | Packed BCD | 7-bit ASCII |
| 00000000 | 0 | +0 | +0 | 0 | 00 | NUL |
| 00000111 | 7 | +7 | +7 | +7 | 07 | BEL |
| 10000000 | 128 | -0 | -127 | -128 | 80 | ERROR |
| 11111110 | 254 | -126 | -1 | -2 | ERROR | ERROR |

1. What is the 16-bit representation of the 2’s complement number 11101010?  
   1110 1010 - 0000 0001 = 1110 1001

1110 1001 -- inverse🡪 0001 0110 = 22

Answer: 1111 1111 1110 1010

1. If propagation delay in a combinatorial circuit is measured in gate delays, how long before all outputs are valid for an 8-bit ripple carry adder circuit?  2\*8+2=18
2. Complete the table to show how the bit string is written in octal or hexadecimal notation.

|  |  |  |
| --- | --- | --- |
| Bit string | Written using octal notation | Written using hexadecimal (0x) notation |
| 110011011111 | 6337 | CDF |
| 010111110001 | 2761 | 5F1 |

1. The 32-bit string 0x01A500FF is stored in little endian byte-addressed memory. Reading from memory starting at the lowest numbered address that contains a byte of this 32-bit string and incrementing the memory address three times will produce what sequence of bytes?  
   FF 00 00 00 00 00 A5 00 00 01 00 00
2. An active high pushbutton switch input circuit has a poorly performing pushbutton characterized by a measured resistance of 100,000 ohms when open (not button is not pushed) and 1000 ohms when closed (the button is pushed). The fixed resistor in this circuit has a measured value of 10,000 ohms. If the reference logic level voltages are +5 volts and 0 volts, what are the voltages of Outputbutton\_pushed and Outputbutton\_not\_pushed?  
   I = U/R = 5/1000+10000

Voutbuttonpushed = I\*10000 = 4.545V

I = U/R = 5/10000+100000

Voutbuttonnotpushed = I\*10000 = 0.4545V

1. Plot the logic signal waveforms for signals In and Out for the following circuit using the supplied graph paper. You must plot the two waveforms for enough time to show how each waveform repeats. When creating your timing plot assume the following:  
   1. At time = 0 ns (nanoseconds, 10^-9 second), the logic level at circuit node In = 1, and the logic level at Out = 1. The nodes In and Out are, respectively, the place of input to gate NOT1 and the place of output of NOT1. There is zero propagation delay between In and NOT1 input, nor any propagation delay between NOT1 and Out.
   2. The propagation delay of the gate NOT1 itself is *T* ns where *T* is either (a) the number of letters in the spelling of your preferred first name as shown in Blackboard or (b) the decimal number 9 if the number of letters from part (a) is 10 or more. [Across all students in the class, we will solve a set of related versions of this question.]  
        
      Type the name you are using to determine the NOT1 propagation delay that you will use when answering this question here \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.  
      Enter the number of letters in your name or 9, per instructions above, here \_\_\_\_\_\_ .
   3. The propagation delay through the wire from node Out to node In is *S* ns where *S* is defined as follows. If your lab session is on Tuesday, then *S* = 2. If your lab session is on Wednesday, then *S* = 3. If your lab session is on Thursday, then *S* = 4. If your lab session is on Friday, then *S* = 5.  
      Enter your value for *S* here \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ .  
        
       

